GAURAV VERMA

PCB analysis| VLSI | FPGA | Python | Verilog | Matlab
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INDUSTRY EXPERIENCE

- Product Validation Engineer at Cadence Design Systems, NSEZ, Noida.
  (May 2022 – Till date)
  - MTBF analysis of PCB (including schematic design)
  - Thermal analysis of PCB (completely routed board)
  - Automations, Regression Management

EDUCATION

Qualification	Year	Board / University	Score
PhD (VLSI)	2019-2024	ECE Department, IIT Roorkee	7.5 CGPA
M.Tech (VLSI Design)	2019	CDAC Mohali (IKG-PTU)	7.72 CGPA
B. Tech (Electronics)	2017	BCAS, University of Delhi	85.89%
Senior School	2012	RLB School, CBSE	94.20%
High School	2010	RLB School, CBSE	10 CGPA

ACHIEVEMENTS AND CERTIFICATIONS

- GATE 2017 Score of 259 and GATE 2019 Score of 369 in EC domain.

SOFTWARE PROFICIENCY

- Scripting : Basic and advanced Linux systems across different OS
- VLSI : Cadence Virtuoso, Xilinx ISE, FPGA (Sparton, Zed board)
- Coding : VHDL, Verilog, System Verilog, UVM
- Programming : C++, Python
- Electronics : Proteus Design Suite, Arduino IDE, QUCS, Eagle, PSPICE, Octave

PUBLICATIONS

Journals:

[1] G. Verma, S. Soni, A. Nisar, and B. K. Kaushik, 'Multi-bit MRAM based High Performance Neuromorphic Accelerator for Image Classification' Neuromorphic Computing and Engineering, 2024.

[2] S. Shreya, G. Verma, S. N. Piramanayagam, and B. K. Kaushik, "Energy-efficient all-spin BNN using voltage-controlled spin-orbit torque device for digit recognition," IEEE Trans. Electron Devices, vol. 68, no. 1, pp. 385-392, 2021.

[3] G. Verma, S. Soni, A. Nisar, S. Dhull, and B. K. Kaushik, 'Energy Efficient CNN Accelerator Using Voltage Gated DSHE-MRAM', IEEE Trans. Electron Devices.

[4] A. Nisar, H. Nehete, G. Verma, and B. K. Kaushik, "Hybrid multilevel STT/DSHE memory for efficient CNN training," IEEE Trans. Electron Devices, vol. 70, no. 3, pp. 1006-1013, 2023.

[5] S. Soni, G. Verma, and B. K. Kaushik, "Energy efficient ternary computation unit using DSHE-MRAM," IoP Semiconductor Science and Technology (SST), vol. 38, no. 2, pp. 025005, 2022.

[6] S. Soni, G. Verma, H. Nehete, and B. K. Kaushik, "Energy-efficient spin-based implementation of neuromorphic functions in CNNs," IEEE Open Journal of Nanotechnology, vol. 4, pp. 102-108, 2023.

[7] G. Verma, N. Bindal, A. Nisar, S. Dhull, and B. K. Kaushik, "Advances in Neuromorphic Spin-Based Spiking Neural Networks: A Review," IEEE Nanotechnology Magazine, vol. 15, no. 5, 2021.

[8] G. Verma, A. Nisar, S. Dhull, A. Prajapati, and B. K. Kaushik, "Neuromorphic accelerator for spiking neural networks using SOT-MRAM crossbars," IEEE Trans. Electron Devices, 2022.

[9] G. Verma, S. Soni, and B. K. Kaushik, "Spin based image edge detection in spiking and non-spiking domains," IoP Nanotechnology, vol. 35, no. 5, pp. 055201, 2023.

International Conferences:

[1] G. Verma, A. Prajapati, N. Bindal, and B. K. Kaushik, "Comparative analysis of spin based memories for neuromorphic computing," in Proc. SPIE International Symposium on Nanoscience + Engineering, Spintronics XIII, San Diego, CA, USA, vol. 11470, Aug 2020.

[2] H. Nehete, G. Verma, A. Gupta, P. Kaushik, and B. K. Kaushik, "FPGA based CNN accelerator for high-speed biomedical application," in Proc. High-speed biomedical imaging and spectroscopy VIII, 12390, pp. 65-74, 2023.

[3] S. Soni, G. Verma, A. K. Shukla, and B. K. Kaushik, "Energy efficient DSHE based analogue multiply accumulate computing crossbar architecture," in Proc. APCCAS, 2023.

[4] A. Sehgal, G. Verma, S. Dhull, S. Roy, B. K. Kaushik, "Analysis of advanced STDP for neuromorphic computing using MRAM," in Proc. IEEE Nanotechnology Materials and Devices Conf., Paestum, Italy, NMDC, 2023.

PROJECTS

- **JRF project on spintronic memories, circuits and architectures**

Magnetic random-access memory for multi-level bitcell design and its application at circuit and algorithm level.

- **FPGA implementation of neural network for image and video processing**

Block level design and HDL IP design for image edge detection for HDMI based video streaming implemented on ZYNQ and PYNQ processor boards using Vivado.

- **Dual port BRAM read write operation on Vivado (2021)**

This involves implementing the inbuilt BRAM module with single and dual port functionality for read and write operation.

- **IP integrator for basic GPIO on Zedboard (2021)**

This involves implementing the self-created IP core with Zynq processor to control the input-output entities on hardware.

- **DNN architectures with AlexNet / VGG16 / ImageNet with MNIST / CIFAR datasets (2020)**

This involves implementing the various models available with datasets to apply CNN concept with quantization and pruning techniques.

- **FPGA Implementation of Image Processing Techniques (2019)**

This involves HDL code generation from Matlab Code and masking concept is implemented. The code includes conversion of image to text and text to image conversion.

- **Classification of Rice Crop infection using Image Processing (2018-19)**

The project aims at classification of two diseases namely Rice Hispa and Stem Borer using Neural Networks. Matlab software version 2018b is used for coding, training and testing purpose.

- **DST – SERB Project (2018-19)**

I worked for a year under the Project by Department of Science and Technology which focuses on use of Foldscope based image acquisition at CDAC Mohali.

- **Wireless Communication system using LED Array and Solar Panel (2018)**

This project deals with the concept of Light Fidelity and its application for underwater communication. The transmitter had LED array and receiver had solar panel. I worked for about 6 months with my senior on the project which successfully transmitted a 5 KB document across 2 meters distance through water.

- **FSM based UART module (2018)**

This project involves basic Finite State Machine based design of Universal Asynchronous Receiver Transmitter module which involves 8 bit data transfer at baud rate of 9600.

AWARDS

"Deepika Wangaroo Memorial Prize" awarded by Bhaskaracharya College of Applied Science for academics during graduation.

ACHIEVEMENTS AND CERTIFICATES

- "**VLSI Devices and Technology**", EICT, IIT Roorkee, 8-12 Jan, 2018
- **Technology based Entrepreneurship Development Program TEDP** in IT, Sponsored by DST, Oct 3 – Nov 14 2018
- "**Imaging Application through MATLAB**", EICT, IIT Roorkee, 09-13 Oct, 2018
- "**Wireless and Mobile Communication**" through NKN under Scheme of financial assistance for setting up of EICT Academics of MeitY, IIT Guwahati, 3-7 Dec, 2018
- "**Introduction to Programming in C**", NPTEL Online Certification, 20 hour Course, IIT Kanpur, September 2015
- "**VLSI Technology**", NPTEL Online Certification, 40 hour Course, IIT Madras, May 2015

KEY INTERESTS

Cooking, Movies, Lawn Tennis

LANGUAGE PROFICIENCY

English Hindi

PERSONAL DETAILS

Date of Birth : 02 July 1994

Residential Address : House number 1103/1, A block Indira Nagar Lucknow, Uttar Pradesh – 226016